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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAVIS, JOHN Q	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,628	BUNDY ET AL.	
	Examiner	Art Unit	
	John Chavis	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-22 and 24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result. No physical transformation is recited and additionally, the final result of the claim is executable code (software) comprising descriptive material (wherein…) or a compiler (software), capable or providing various functions, which is not a tangible result because the claimed software is not directed toward a process (method), a machine (an apparatus or system with specific hardware components specified), a manufacture (for example, a computer storage medium comprising various interacting functions) or a composition of matter.

Claim 1 **still** appears to be directed toward software (a test development tool) via his program code for accessing, and his test development program code for evaluating and determining. Nothing in the claim recites statutory component that would indicate that the development tool is anything other than software. **The applicant added "computer readable medium…"; however, sect. 0088 of the applicant's specifications indicates that computer readable mediums can be any means that**

can propagate or transport data. Therefore, the claims are not considered to exclude for example a carrier wave that is deemed non statutory. Furthermore, everything else in the claim is considered to define a program that is also deemed non-statutory. The dependent claims do not cure the issues associated with their respective parent claims.

The features of claim 18 have the same type of issues as claim 1 with its code for evaluating, determining, combining, testing and providing. The dependent claims do not cure the issues associated with their respective parent claims.

In reference to claim 21, the claim recites a system and what is expected is hardware components that are interconnected to define the system. However, what is provided is the same type of components listed in claims 1 and 18. The only difference is the “means for” phrase placed in front of the components. However, it is not clear that the “means for” are anything other than the code claimed in the previous claims above. **This rejection is still considered proper because "accessing", “evaluating” and “defining”, as specified above can be provided for without a computer (system). What is expected is components that clearly link the system to statutory components of a computer or other statutory system (such as a processor, a tangible storage device, etc.)** Furthermore, it is not clear that the means for defining cure the problems specified above. The components of claim 22 are considered to provide support for the assessment that specifies that claim 21 is merely software; however, the components appear to be disassociated from the other components and also do not appear to be utilized (just merely mentioned).

The computer readable medium of claim 24 is rejected via sects. 0088-0089. The claims are directed to a signal directly or indirectly by claiming a medium and the Specification recites evidence where the computer readable medium is defined as a "***wave"*** (such as a carrier wave). In that event, the claims are directed to a form of energy which at present the office feels does not fall into a category of invention. Section 0088 indicate that the computer readable medium can be any means that can communicate, propagate or transport the program. Then, in sect. 0089 he specifies that the medium could even be "paper". **The computer readable medium has previously been addressed above in reference to this claim and is further addressed in reference to claim 1. Therefore, it will not be further discussed here. Furthermore, a non statutory computer readable medium and program code (software per se) is not considered sufficient to define an apparatus (hardware). Therefore, this claim is also considered to still be non statutory. Therefore, in none of the claim has an algorithm as well as a general purpose computer or microprocessor been defined.**

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10, 12-15, 18-19, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (7,290,174) in view of Hamameh et al. (2004/0015870). **This action is also hereby repeated since this rejection is also still considered proper. The applicant claims that the feature of accessing "pre existing programs" does not exist in either reference; however, Gray teach the feature in col. 4 lines 26-34, which identifies (not creates, therefore accessing pre existing…) test fragments and arrange them in different combinations (allowing for combination into new programs) to generate test sequences. He further provides for evaluating in col. 5 lines 1-31.**

Hamameh provides for the features via fig. 4 via his step 248 (store test procedures. i.e. "ones that are pre established) and identifies one or more alternate products for the sub elements via selections (steps 250-251, which also are pre existing since they are not defined as being generated), see also fig. 5 steps 310 and 312. See also col. 1 lines 18-24 (which provides for integrating different software products (for example, pre-existing test programs) and using retrieved test codes (again pre-existing) to test integration (col. 2 lines 13-31). Note also how testing code and tables (I.E. pre-existing) are modular (can be reused) and can be combined to generate new functionality (see col. 6 lines 14-43, col. 7 line 1-17 and col. 8 line 15-35).

Claims 1. A test development tool (see the title and the abstract) comprising: test development program code for accessing first and second pre-established test

programs (see the “disparate devices in col. 1 lines 13-23), each of said first and second pre-established test programs having been previously established for respective first and second pre-existing integrated circuit devices (see again the citations above),

Although the features above are considered to represent that the features of the first and second test programs are established for pre-existing Integrated circuit devices, the feature may not be clearly specified in Gray’s system. However, the feature is specified in Hamameh’s system to enable efficient integration testing. Therefore, It would have been obvious to a person having ordinary skill in the art at the time of the invention to modify Gray’s system with the integration testing feature of Hamameh’s system for the seme reason it is utilized by Hamameh to make the integration more compatible and efficient, see the title, abstract, col. 2 lines 12-20, col. 2 lines 54-64, col. 4 lines 19-31, col. 7 lines 36-61 and col. 8 lines 23-35.

and said first and second pre-established test programs each having respective first and second sets of subtest code portions (see the fragments in col. 1 lines 41-49); test development program code for evaluating the first and second sets of subtest code portions and determining whether any respective subtest code portions of said first and second sets of subtest code portions have features allowing for combination in a new test program (see col. 1 lines 50-60), said test development program code for the evaluating and determining steps providing at least one output result thereof (see col. 4 lines 47-58, which specifies that the combinations can be in a variety of different

manners); test development program code for defining a new test program including at least one new subtest code portion for concurrently testing first and second pre-existing integrated circuit devices using the at least one output result of the evaluating and determining steps (see the cited portions above and col. 3 line 64-col. 4 line 14).

2. A test development tool according to claim 1, in which the at least one new subtest code portion for concurrently testing provides for faster overall device test execution (see col. 8 lines 33-38, especially the efficient and effective mechanisms).

3. A test development tool according to claim 1 which further includes: test development program code for prompting a user to participate in the evaluating and determining steps of the subtest code portions of the first and second pre-established test programs (see col. 7 lines 16-42 and col. 8 lines 1-4).

4. A test development tool according to claim 1 wherein said features allowing for combination comprise respective subtest code portions from each of said first and second pre-established test programs which are substantially operatively compatible (note that the system provides for verification and physical design testing, see col. 8 lines 35-53).

5. A test development tool according to claim 4 wherein said subtest code portions having features allowing for combination are defined in said defining step as a single set

of subtest code portions to be performed via a common port in a multi-port testing environment (see col. 3 lines 40-43 and col. 4 lines 47-58).

6. A test development tool according to claim 5 wherein said features allowing for combination are selected from the group consisting of clocks and common pins (see col. 8 lines 39-53).

7. A test development tool according to claim 1 wherein said features allowing for combination comprise respective subtest code portions from each of said first and second pre-established test programs which are mutually exclusive, yet provide for concurrent operation via discrete first and second ports (see col. 4 lines 47-58).

8. A test development tool according to claim 7 wherein the respective subtest code portions from each of said first and second pre-established test programs are evaluated for time of operation (see col. 8 lines 33-53).

9. A test development tool according to claim 8 which further includes: test development program code for prompting a user to participate in the evaluation of the timing of the subtest code portions of the first and second pre-established test programs (see the cited portions above and col. 8 lines 1-4).

10. A test development tool according to claim 8 wherein the respective subtest code

portions from each of said first and second pre-established test programs are matched with each other based upon the similarity of their respective times of operation (see col. 4 lines 47-58).

12. A test development tool according to claim 1 wherein the respective subtest code portions from each of said first and second pre-established test programs are evaluated for new subtest code portion sequencing (see the rejection of claim 1).

13. A test development tool according to claim 12 wherein the respective subtest code portions from each of said first and second pre-established test programs are matched with each other to create respective new subtest code portions and are placed into a new test flow as a result of the subtest sequencing evaluation (see again the rejection of claim 1).

14. A test development tool according to claim 12 wherein the respective subtest code portions from each of said first and second pre-established test programs are matched with each other to create respective new subtest code portions and are placed into a new test flow as a result of the subtest sequencing evaluation and based upon one of the testflows from one of the first and second pre-established test programs (see the rejections of claims 5-6).

15. A test development tool according to claim 12 which further includes: test

development program code for prompting a user to participate in the sequencing of the new subtest code portions (see the rejections of claims 5-6).

18. A test development tool comprising: test development program code for evaluating relative timings of first and second sets of subtest code portions of first and second pre-established test programs and determining an organization for a combination of respective subtest code portions of said first and second sets of subtest code portions, said test development program code for the evaluating and determining steps providing at least one output result thereof, each of said first and second pre-established test programs having been previously established for respective first and second pre-existing integrated circuit devices; test development program code for combining subtest code portions, including combining the separate setups of vectors, timings and levels from the respective first and second sets of subtest code portions for the subtest code portions being combined and defining a new combined overall test program including at least one new combined subtest code portion for concurrently testing first and second pre-existing integrated circuit devices using the at least one output result of the evaluating and determining steps; and, test development program code for providing at least one test method to run the at least one new combined subtest code portion of the new combined overall test program for a new combination device including the first and second pre-existing integrated circuit devices.

19. A test development tool according to claim 18 further comprising test development

program code for defining port assignments for the pins of the new combination device (see col. 8 lines 48-53).

21. A system comprising: means for accessing a plurality of pre-established test programs, said plurality of pre-established test programs each having subtest code portions and each having been previously established for respective pre-existing integrated circuit devices; means for evaluating the test code portions of each of said plurality of pre-established test programs and for determining whether any subtest code portions of each of the respective pre-established test programs are operatively compatible, said means for evaluating and determining providing an output result of the evaluation and determination; means for defining a new test program including at least one new subtest code portion using the output result of the evaluation and determination (see the rejection of claim 1).

22. A system according to claim 21 which further includes automated test equipment including test development hardware, firmware and software (see again the rejection of claim 1).

23. A method comprising: accessing first and second pre-established test programs in a multi-port concurrent test environment, each of said first and second pre-established test programs having been previously established for respective first and second pre-existing integrated circuit devices, and said first and second pre-established test

programs each having respective first and second sets of subtest code portions; evaluating the first and second sets of subtest code portions and determining whether any respective subtest code portions of said first and second sets of subtest code portions have features allowing for combination into a new subtest code portion in a new test program, said evaluating and determining steps providing at least one output result thereof; defining a new test program including a new subtest code portion for concurrently testing first and second pre-existing integrated circuit devices using the at least one output result of the evaluating and determining steps (see the rejection of claim 1).

24. Apparatus comprising: a computer readable medium; wherein a computer program is stored on the computer readable medium, the computer readable medium being adapted for developing at least a portion of an integrated circuit test in a concurrent multi-port automated test environment; said computer program comprising: program code to access first and second pre-established test programs and to access respective first and second subtest code portions of the first and second pre-established test programs; program code to evaluate whether any of the respective first and second subtest code portions of the respective first and second pre-established test programs may be combined to create a new subtest code portion in a new test program, said program code to evaluate providing at least one output result thereof; and program code to define a new subtest code portion of a new test program using the at least one output result of the program code to evaluate (see the rejection of claim 1).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Chavis whose telephone number is (571) 272-3720. The examiner can normally be reached on M-F, 9:00am-5:30pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JC/

/John Chavis/
Primary Examiner, Art Unit 2193